IN THE SPECIFICATION

Please substitute the following paragraph(s) for like numbered paragraphs of the specification:

[0035] Figure 13 is a timing diagram showing exemplary control and data signals during a read operation within the circuit arrangement of Figure 12. Initially, at time T1, the precharge signal 543 (PRE) goes low for a predetermined interval to precharge the bit lines 524 and 526 to supply voltage levels. As discussed, an always-on precharge circuit may be provided to maintain the precharged state of the bit lines 524 and 526 after the precharge signal 543 is deasserted (e.g., to a high state). At time T2, a word line (WL) is activated to enable an address-selected one of the CAM cells 521 to drive a differential signal onto the bit lines 524 and 526. At time T3, the sense amp bit select signal 547 (SABS) goes high to switch on transistors 531 and 533, thereby forming a path between the gate terminals of transistors 525 and 527 and the bit lines 526 and 524, respectively. Also, at or before time T3, the sense amp pull-up control signal 545 (SAPUC) goes high to switch the local precharge transistors 535 and 537 and the sense amp enable transistor to a substantially non-conducting state. By this operation, the voltage levels at the gate terminals of transistors 525 and 527 differentiate according to the states of the corresponding bit lines 526 and 524. Consequently, when the sense amp pull-up control signal 545 is asserted (i.e., goes low) at time T4, the enable transistor 529 is switched on (i.e., by operation of inverter 549) to enable transistors 525 and 527 to latch the states of the bit lines 524 and 526 at rail-to-rail differential potentials. At time T5, the sense amp bit select signal 547 is deasserted to isolate the latching sense amplifier 523 from the bit lines 524 and 526, thereby retaining the rail-to-rail differential potentials of the bit lines 524 and 526 at the drain terminals of transistors 525 and 527, but permitting the word line (WL) to be deasserted and the bit lines 524 and 526 to be precharged. At time T6, the word line is deactivated to enable the bit lines to be precharged in preparation for a subsequent read or write operation. Note that the latched state of the latching sense amplifier 523 will remain until the next rising edge of the sense amp pull signal 545. Accordingly, the latched nodes of the latching sense amplifier 523 (i.e., drain terminals of transistors 525 and 527) may be used to drive logic level circuits (e.g., for output from the CAM device or for storage in other registers or circuits of the CAM device) even as the bit lines 524 and 526 are precharged in preparation for a subsequent data access operation.